MCA-02

December - Examination 2015

MCA Ist Year Examination

Digital Logic

Paper - MCA-02

Time : 3 Hours] **[Max. Marks :- 80**

Note: The question paper is divided into three sections A, B and C. Write answers as per given instructions.

Section - A

8 x 2 = 16

(Very Short Answer Questions)

Note: Answer **all** questions. As per the nature of the question delimit your answer in one word, one sentence or maximum upto 30 words. Each question carries 2 marks.

1) (i) What is don't care condition?

(ii) What is statement of De-morgon's theorem?

(iii) What is full form of EBCDIC?

(iv) What is form factor?

(v) Write any two types of BOOLEAN operators.

(vi) What is meaning of floating point representation?

(vii) Write any two benefits of karnaugh map?

(viii) What is RAM?

Section - B

$4 \times 8 = 32$

(Short Answer Questions)

Note: Answer any **four** questions. Each answer should not exceed 200 words. Each question carries 8 marks.

2) Discuss the 4-bit binary parallel adder.

3) How 3 × 8 line decoder works?

4) Discuss duality property with any Boolean expression.

5) Explain organization of simple ROM cell.

6) Discuss parallel-in-parallel-out register.

7) Describe RS flip flop with suitable diagram and functionality.

8) Describe half adder and full adder with diagram and truth tables.

9) Explain the universal gate property of NAND gate for XOR, OR gate formation?

Section - C

$2 \times 16 = 32$

(Long Answer Questions)

Note: Answer any **two** questions. You have to delimit your each answer maximum upto 500 words. Each question carries 16 marks.

10) Design a 4-bit serial-in-serial-out shift register with neat sketch.

11) Explain the working and detailed classification of parallel to serial converter.

12) Write a short note on:
    (i) Counter
    (ii) Static RAM

13) Explain the working of tri state TTL NAND gate.

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